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CLAIMS

1. A clock synchronizer generating a second clock signal (FCLK) synchronized with a first clock signal (RCLK), comprising:

a phase difference detection circuit (1) detecting a phase difference between said first and second clock signals (RCLK, FCLK), and setting a first control signal (UP, DOWN) to be at an activated level for a time period corresponding to the phase difference;

a loop filter (9) connected to a predetermined node;

a current-supply circuit (2, 7, 8, 41, 80, 86, 87, 110, 113) supplying current to said loop filter (9) in response to the first control signal (UP, DOWN) from said phase difference detection circuit (1); and

a clock generating circuit (12, 13, 40) generating said second clock signal (FCLK) in accordance with a potential (VC) of said predetermined node;

said current-supply circuit (2, 7, 8, 41, 80, 86, 87, 110, 113) including

a variable current source (2a, 2b, 41a, 41b, 80a, 80b, 110a, 110b, 113a, 113b) whose output current can be controlled,

a first switching circuit (4, 5, 82, 83) passing output current of said variable current source (2a, 2b, 41a, 41b, 80a, 80b, 110a, 110b, 113a, 113b) through said loop filter (9) in response to that said first signal (UP, DOWN) is set to be at the activated level, and

a first control circuit (7, 8, 86, 87) controlling said variable current source (2a, 2b, 41a, 41b, 80a, 80b, 110a, 110b, 113a, 113b) such that predetermined constant current flows from said variable current source (2a, 2b, 41a, 41b, 80a, 80b, 110a, 110b, 113a, 113b) to said loop filter (9), based on the potential (VC) of said predetermined node.

2. The clock synchronizer according to claim 1, wherein

said variable current source (2a, 2b, 41a, 41b, 80a, 80b, 110a, 110b, 113a, 113b) includes a first transistor (3, 6) of a first conductivity type whose input electrode receives a first control potential (VCP, VCN),

said first switching circuit (4, 5, 82, 83) connects said first transistor

(3, 6) between a line of a first power-supply potential (VCC, GND) and said loop filter (9) in response to that said first control signal (UP, DOWN) is set to be at the activated level, and

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said first control circuit (7, 8, 50, 51, 86, 87) controls said first control potential (VCP, VCN) such that predetermined constant current flows through said first transistor (3, 6) connected between the line of said first power-supply potential (VCC, GND) and said loop filter (9), based on the potential (VC) of said predetermined node.

3. The clock synchronizer according to claim 2, wherein

Fig 1

said first control circuit (7, 8, 50, 51) includes

a second transistor (21, 26) of a first conductivity type whose first electrode is connected to the line of said first power-supply potential (VCC, GND), and whose input electrode is connected to a second electrode of said second transistor, and outputting said first control potential (VCP, VCN) from the second electrode,

a third transistor (22, 25) of a second conductivity type whose first electrode is connected to a second electrode of said second transistor (21, 26) and whose input electrode receives the potential (VC) of said predetermined node, and

a first resistance element (23, 24) connected between a second electrode of said third transistor (22, 25) and a line of a second power-supply potential (GND, VCC).

4. The clock synchronizer according to claim 3, wherein said first control circuit (50, 51) further includes a second resistance element (52, 53) connected between the second electrode of said second transistor (21, 26) and the line of said second power-supply potential (GND, VCC).

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5. The clock synchronizer according to claim 3, wherein said variable current source (41a, 41b) further includes a fourth transistor (42, 43) of a first conductivity type, connected in parallel with said first transistor (3, 6), whose input electrode receives a constant bias potential

(VBP, VBN).

6. The clock synchronizer according to claim 2, comprising:

a lock detection circuit (85) detecting whether or not the phase difference between said first and second clock signals (RCLK, FCLK) is smaller than a predetermined level, setting a lock detection signal (ϕL) to be at an activated level when it is smaller, and setting said lock detection signal (ϕL) to be at an inactivated level when it is larger,

Species II Fig 17

said variable current source (80a, 80b) further including a second transistor (81, 84) of a first conductivity type whose input electrode receives a constant bias potential (VBP, VBN),

said first switching circuit (4, 5, 82, 83) connecting said first transistor (3, 6) between the line of said first power-supply potential (VCC, GND) and said loop filter (9) when said lock detection signal (ϕL) is at an activated level, and connecting said second transistor (81, 84) between the line of said first power-supply potential (VCC, GND) and said loop filter (9) when said lock detection signal (ϕL) is at an inactivated level, in response to that said first control signal (UP, DOWN) is set to be at an activated level.

7. The clock synchronizer according to claim 2, further comprising:

a lock detection circuit (85) detecting whether or not the phase difference between said first and second clock signals (RCLK, FCLK) is smaller than a predetermined level, setting a lock detection signal (ϕL) to be at an activated level when it is smaller, and setting said lock detection signal (ϕL) to be at an inactivated level when it is larger,

Species III Fig 18

said variable current source (80a, 80b) further including a second transistor (81, 84) of a first conductivity type whose input electrode receives a second control potential (VCP', VCN'),

said first switching circuit (4, 5, 82, 83) connecting said first transistor (3, 6) between the line of said first power-supply potential (VCC, GND) and said loop filter (9) when said lock detection signal (ϕL) is at an activated level, and connecting said second transistor (81, 84) between the line of said first power-supply potential (VCC, GND) and said loop filter (9) when said lock detection signal (ϕL) is at an inactivated level, in response to that said first control signal (UP, DOWN) is set to be at an activated level.

line of said first power-supply potential (VCC, GND) and said loop filter (9) when said lock detection signal (ϕL) is at an inactivated level, in response to that said first control signal (UP, DOWN) is set to be at an activated level,

said current-supply circuit (7, 8, 80, 86, 87) further including a second control circuit (86, 87) controlling said second control potential (VCP', VCN') such that current flowing through said second transistor (81, 84) connected between the line of said first power-supply potential (VCC, GND) and said loop filter (9) is increased in accordance with a potential difference between said first power-supply potential (VCC, GND) and a potential (VC) of said predetermined node, based on the potential (VC) of said predetermined node.

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8. The clock synchronizer according to claim 2, wherein

said first control signal (UP) is a signal for advancing a phase of said second clock signal (FCLK);

said phase difference detection circuit (1) sets said first control signal (UP) to be at an activated level for a time period corresponding to a phase difference between said first and second clock signals (FCLK, RCLK) when the phase of said second clock signal (FCLK) is delayed with respect to said first clock signal (RCLK), sets a second control signal (DOWN) for delaying the phase of said second clock signal (FCLK) to be at an activated level for a time period corresponding to a phase difference between said first and second clock signals (RCLK, FCLK) when the phase of said second clock signal (FCLK) is advanced with respect to said first clock signal (RCLK), and sets said first and second control signals (UP, DOWN) to be at an activated level for a predetermined period of time when phases of said first and second clock signals (RCLK, FCLK) agree with each other; and

said current-supply circuit (2, 7, 8, 41, 80, 86, 87, 110, 113) supplies current of a first polarity to said loop filter (9) in response to that said first control signal (UP) is set to be at an activated level, and also supplies current of a second polarity to said loop filter (9) in response to that said second control signal (DOWN) is set to be at an activated level.

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9. The clock synchronizer according to claim 8, wherein

said variable current source (2a, 2b, 41a, 41b, 80a, 80b, 110a, 110b, 113a, 113b) further includes a second transistor (6) of a second conductivity type whose input electrode receives a second control potential (VCN); and

said current-supply circuit (2, 7, 8, 41, 80, 86, 87, 110, 113) includes

a second switching circuit (5) connecting said second transistor (6) between said loop filter (9) and the line of said second power-supply potential (GND) in response to that said second control signal (DOWN) is set to be at an activated level, and

a second control circuit (8) controlling said second control potential (VCN) such that said predetermined constant current flows through said second transistor (6) connected between said loop filter (9) and the line of said second power-supply potential (GND), based on a potential (VC) of said predetermined node.

10. The clock synchronizer according to claim 9, further comprising a precharge circuit (60) precharging said predetermined node to be at a predetermined potential in response to application of said first and second power-supply potentials (VCC, GND).

11. The clock synchronizer according to claim 8, wherein

said current-supply circuit (2, 7, 8, 41, 80, 86, 87, 110, 113) further includes

a second transistor (6) of a second conductivity type whose input electrode receives a constant bias potential (VBN), and

a second switching circuit (5) connecting said second transistor (6) between said loop filter (9) and the line of said second power-supply potential (GND) in response to that said second control signal (DOWN) is set to be at an activated level.

12. The clock synchronizer according to claim 11, further comprising a precharge circuit (70) precharging said predetermined node to

be at said first power-supply potential (VCC) in response to application of said first and second power-supply potentials (VCC, GND).

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13. The clock synchronizer according to claim 2, wherein

said first control signal (DOWN) is a signal for delaying the phase of said second clock signal (FCLK),

said phase difference detection circuit (1) sets said first control signal (DOWN) to be at an activated level for a time period corresponding to a phase difference between said first and second clock signals (RCLK, FCLK) when the phase of said second clock signal (FCLK) is advanced with respect to said first clock signal (RCLK), sets a second control signal (UP) for advancing the phase of said second clock signal (FCLK) to be at an activated level for a time period corresponding to a phase difference between said first and second clock signals (RCLK, FCLK) when the phase of said second clock signal (FCLK) is delayed with respect to said first clock signal (RCLK), and sets said first and second control signals (DOWN, UP) to be at an activated level for a predetermined period of time when the phases of said first and second clock signals (RCLK, FCLK) agree with each other, and

said current-supply circuit (2, 7, 8, 41, 80, 86, 87, 110, 113) supplies current of a first polarity to said loop filter (9) in response to that said first control signal (DOWN) is set to be at an activated level, and also supplies current of a second polarity to said loop filter (9) in response to that said second control signal (UP) is set to be at an activated level.

14. The clock synchronizer according to claim 13, wherein

said current-supply circuit (2, 7, 8, 41, 80, 86, 87, 110, 113) further includes

a second transistor (3) of a second conductivity type whose input electrode receives a constant bias potential (VBP), and

a second switching circuit (4) connecting said second transistor (3) between said loop filter (9) and the line of said second power-supply potential (VCC), in response to that said second control signal (UP) is set to

be at an activated level.

15. The clock synchronizer according to claim 14, further comprising a precharge circuit (72) precharging said predetermined node to be at said first power-supply potential (GND) in response to application of said first and second power-supply potentials (GND, VCC).

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16. The clock synchronizer according to claim 1, wherein

said variable current source (110a, 110b) includes

a variable potential source (111, 112) whose output potential (V1, V2) can be controlled, and

a transistor (3, 6) whose input electrode receives a constant bias potential (VBP, VBN);

said first switching circuit (4, 5) connects said transistor (3, 6) between an output node of said variable potential source (111, 112) and said loop filter (9), in response to that said first control signal (UP, DOWN) is set to be at an activated level; and

said first control circuit (7, 8) controls said variable potential source (111, 112) such that predetermined constant current flows through said transistor (3, 6) connected between the output node of said variable potential source (111, 112) and said loop filter (9), based on a potential (VC) of said predetermined node.

17. The clock synchronizer according to claim 1, wherein

said variable current source (113a, 113b) includes

a variable potential source (114, 115) whose output potential (V3, V4) can be controlled, and

a transistor (3, 6) whose input electrode receives a constant control potential (VCP, VCN);

said first switching circuit (4, 5) connects said transistor (3, 6) between an output node of said variable potential source (114, 115) and said loop filter (9) in response to that said first control signal (UP, DOWN) is set to be at an activated level; and

said first control circuit (7, 8) controls said control potential (VCP, VCN) and said variable potential source (114, 115) such that predetermined constant current flows through said transistor (3, 6) connected between the output node of said variable potential source (114, 115) and said loop filter (9), based on a potential (VC) of said predetermined node.

18. The clock synchronizer according to claim 1, wherein said loop filter (9) includes a resistance element (10) and a capacitor (11) connected in series between said predetermined node and a line of a reference potential (GND).

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19. A clock synchronizer generating a second clock signal (FCLK) synchronized with a first clock signal (RCLK), comprising:

a phase difference detection circuit (1) detecting a phase difference between said first and second clock signals (RCLK, FCLK) and setting a control signal (UP, DOWN) to be at an activated level for a time period corresponding to the phase difference;

a loop filter (9) connected to a predetermined node;

a current-supply circuit (2, 7, 8, 41, 80, 86, 87, 110, 113) supplying current to said loop filter (9) in response to ~~a~~ the control signal (UP, DOWN) from said phase difference detection circuit (1); and

a clock generating circuit (12, 13, 40) generating said second clock signal (FCLK) in accordance with a control potential (VCP, VCN);

said current-supply circuit (2, 7, 8, 41, 80, 86, 87, 110, 113) including

a transistor (3, 6) whose input electrode receives said control potential (VCP, VCN),

a switching circuit (4, 5) connecting said transistor (3, 6) between a line of a power-supply potential (VCC, GND) and said loop filter (9), in response to that said control signal (UP, DOWN) is set to be at an activated level, and

a control circuit (7, 8, 86, 87) controlling said control potential (VCP, VCN) such that predetermined constant current flows through said

transistor (3, 6) connected between the line of said power-supply potential (VCC, GND) and said loop filter (9), based on a potential (VC) of said predetermined node.

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20. A clock synchronizer generating a second clock signal (FCLK) synchronized with a first clock signal (RCLK), comprising:

a phase difference detection circuit (1) detecting a phase difference between said first and second clock signals (RCLK, FCLK), and setting a control signal (UP, DOWN) to be at an activated level for a time period corresponding to the phase difference;

a loop filter (9) including a resistance element (10) and a capacitor (11) connected in series between a predetermined node and a line of a reference potential (GND);

a current-supply circuit (2, 7, 8, 41, 80, 86, 87, 110, 113) supplying current to said loop filter (9) in response to ~~a~~ control signal (UP, DOWN) from said phase difference detection circuit (1); and

a clock generating circuit (12, 13, 40) generating said second clock signal (FCLK) in accordance with a potential (VC) of said predetermined node;

said current-supply circuit (2, 7, 8, 41, 80, 86, 87, 110, 113) including

a transistor (3, 6) whose input electrode receives a control potential (VCP, VCN),

a switching circuit (4, 5, 82, 83) connecting said transistor (3, 6) between a line of a power-supply potential (VCC, GND) and said loop filter (9), in response to that said control signal (UP, DOWN) is set to be at an activated level, and

a control circuit (7, 8, 86, 87) controlling said control potential (VCP, VCN) such that predetermined constant current flows through said transistor (3, 6) connected between the line of said power-supply potential (VCC, GND) and said loop filter (9), based on a potential (VC') of a node between said resistance element (10) and ~~a~~ capacitor (11).